

FIG. 1

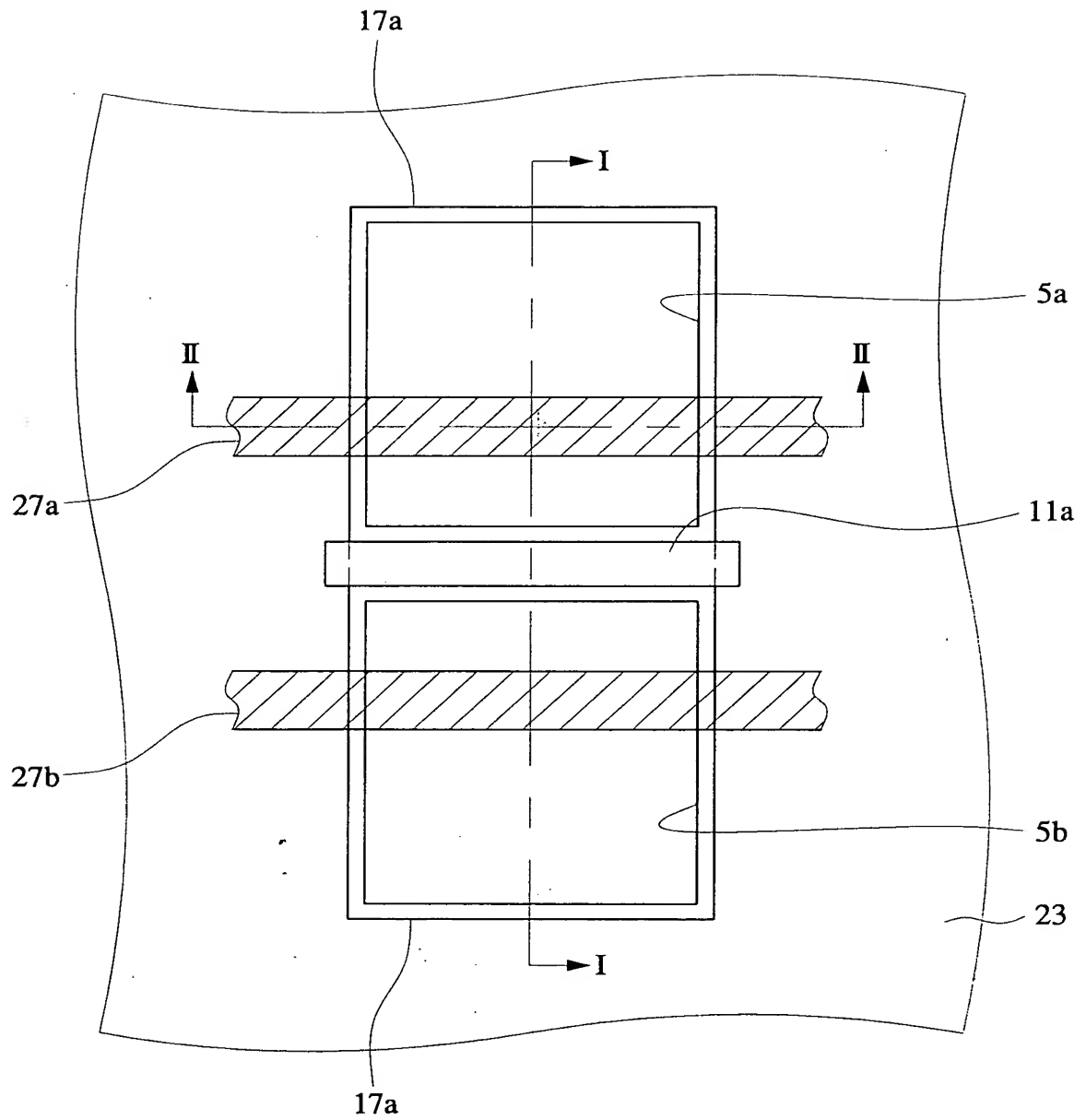


FIG. 2A

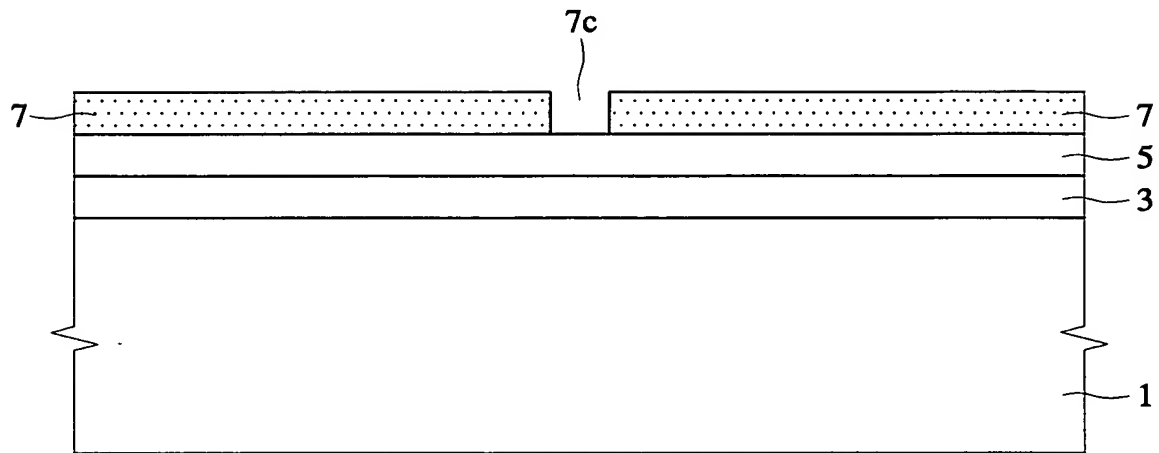


FIG. 2B

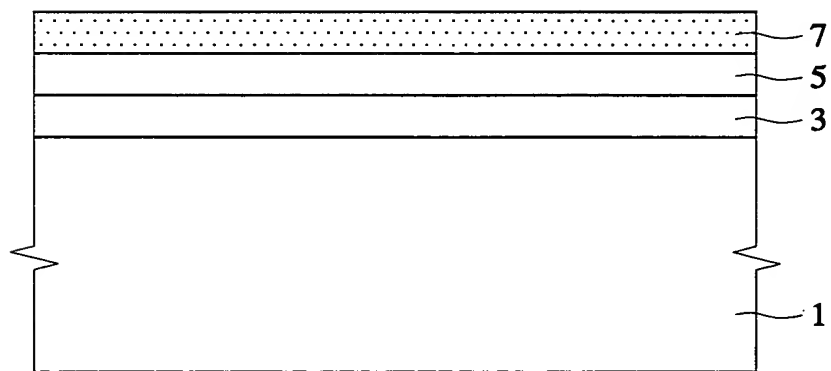




FIG. 4A

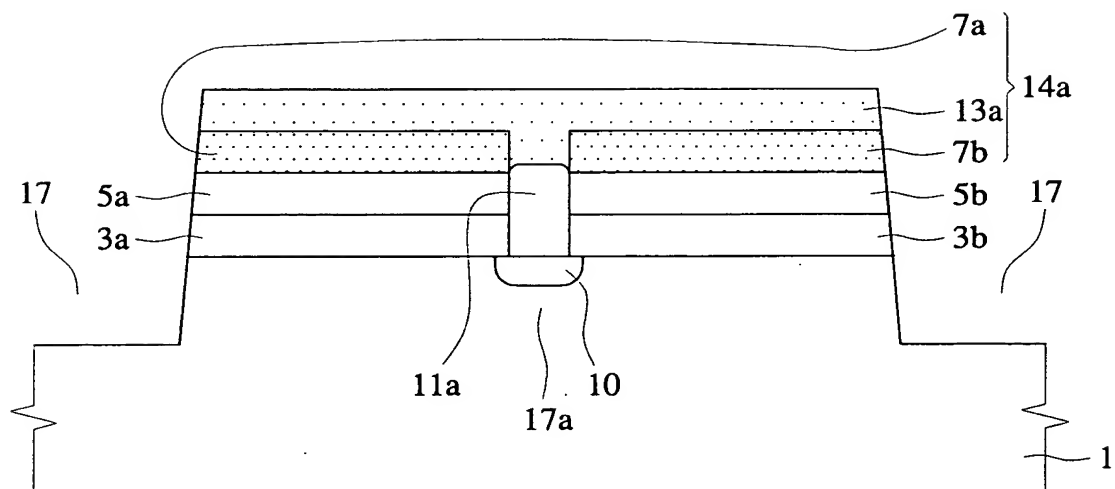


FIG. 4B

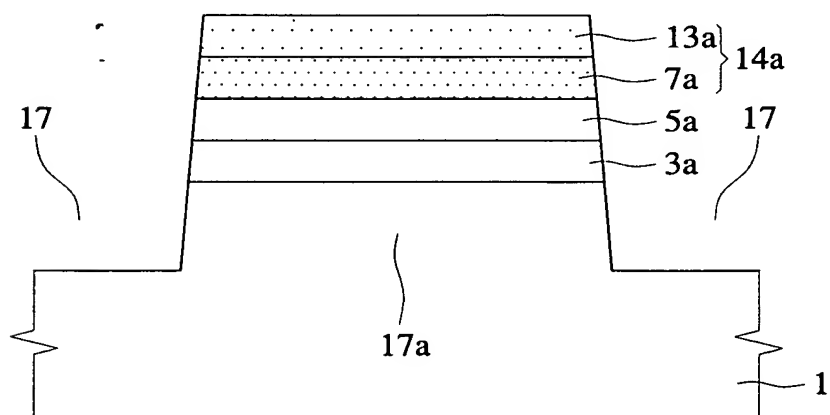


FIG. 5A

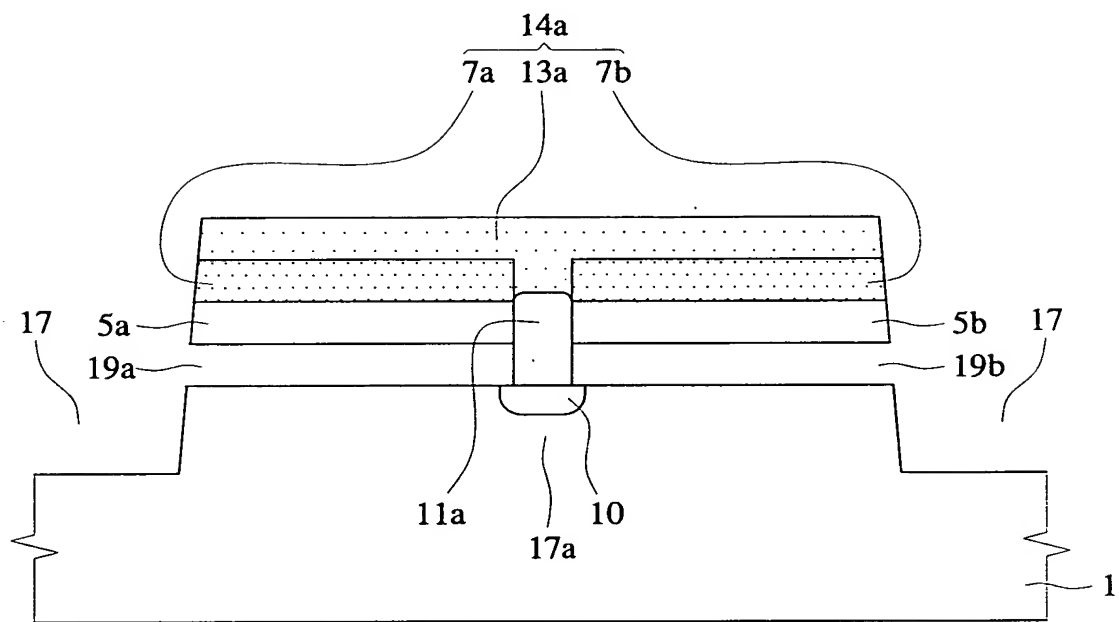


FIG. 5B

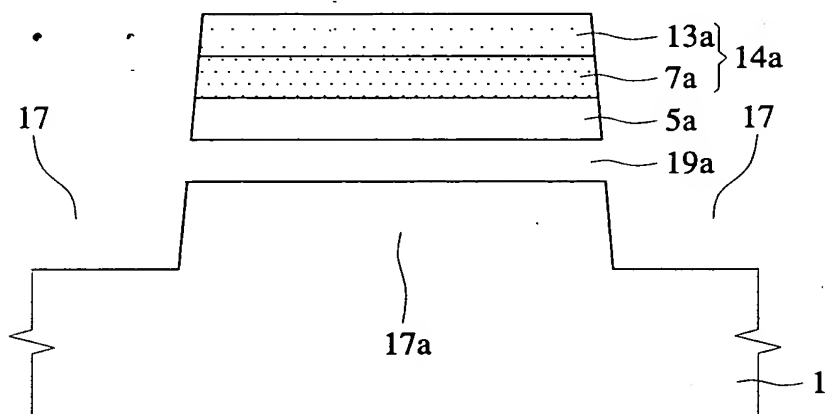


FIG. 6A

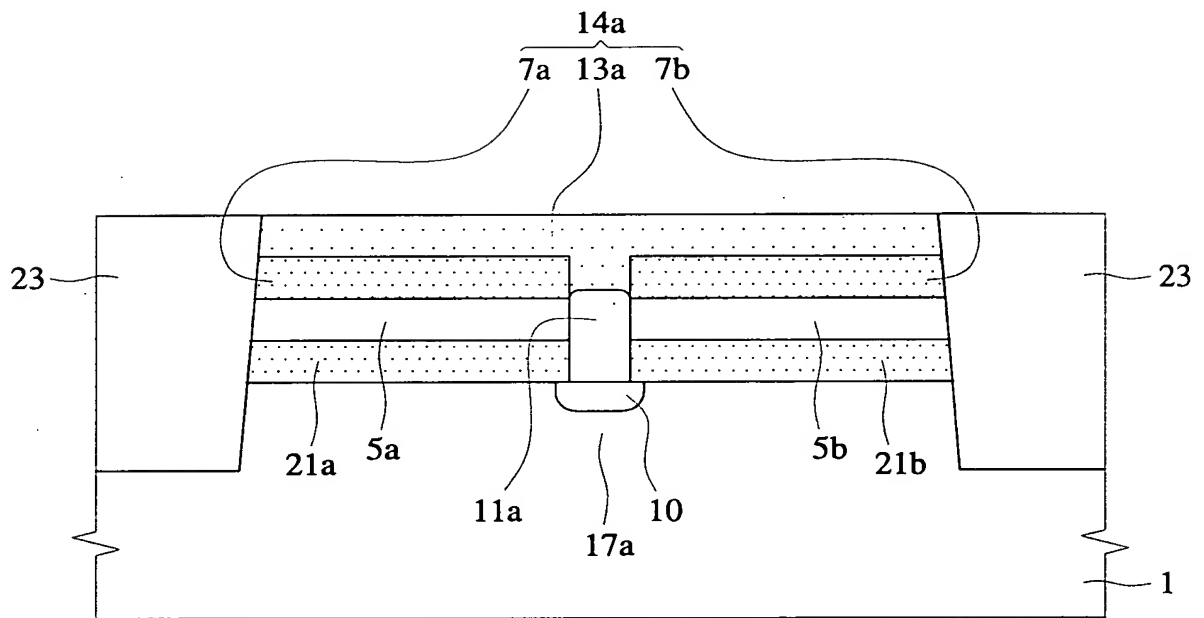


FIG. 6B

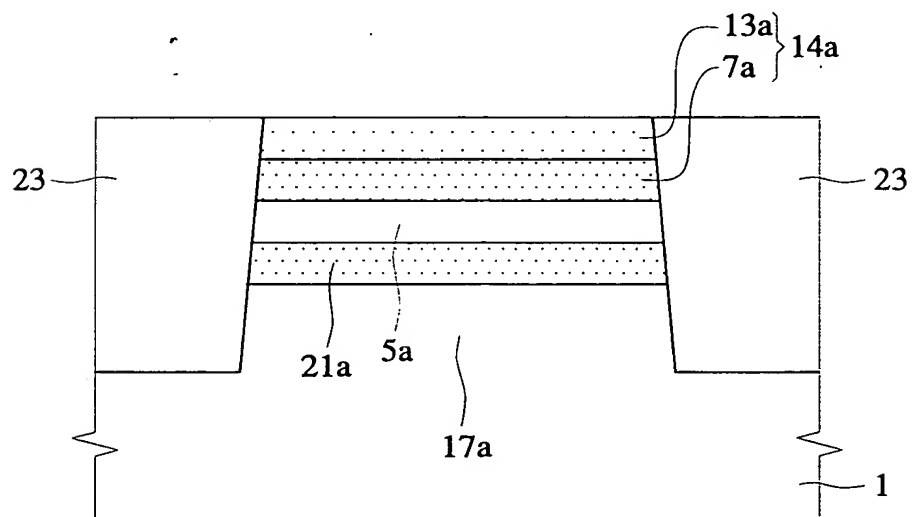


FIG. 7A

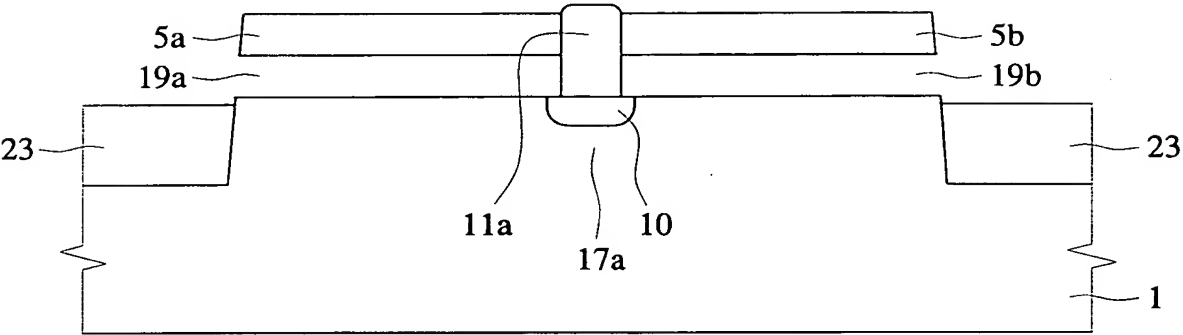


FIG. 7B

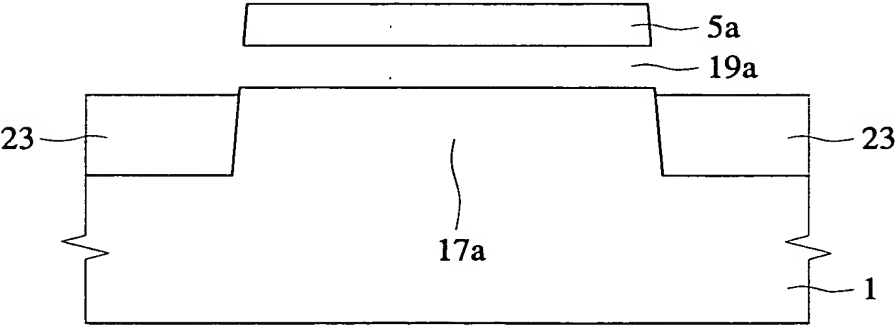


FIG. 8A

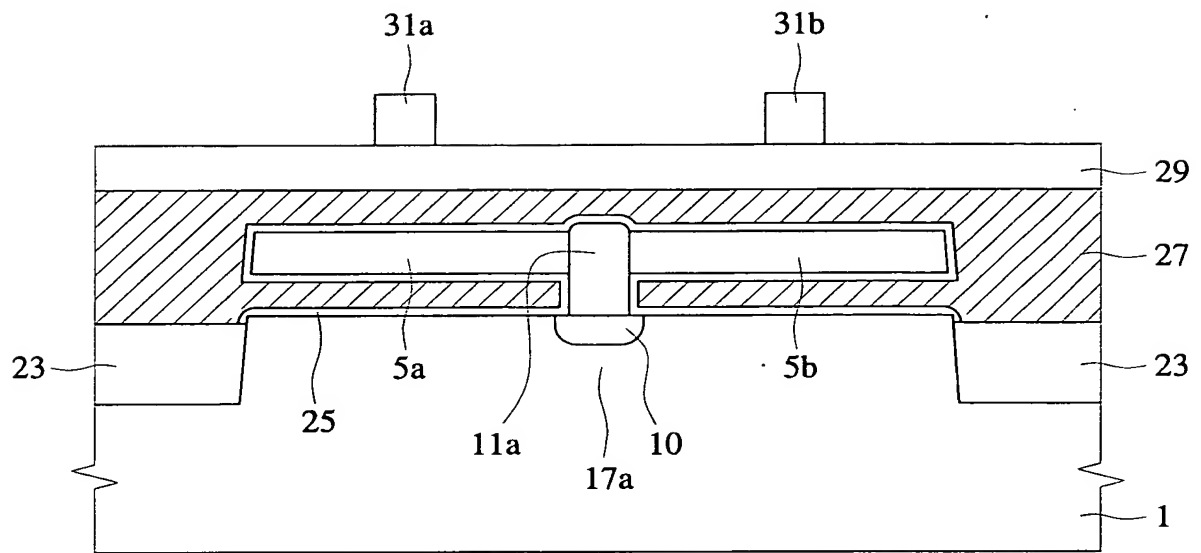


FIG. 8B

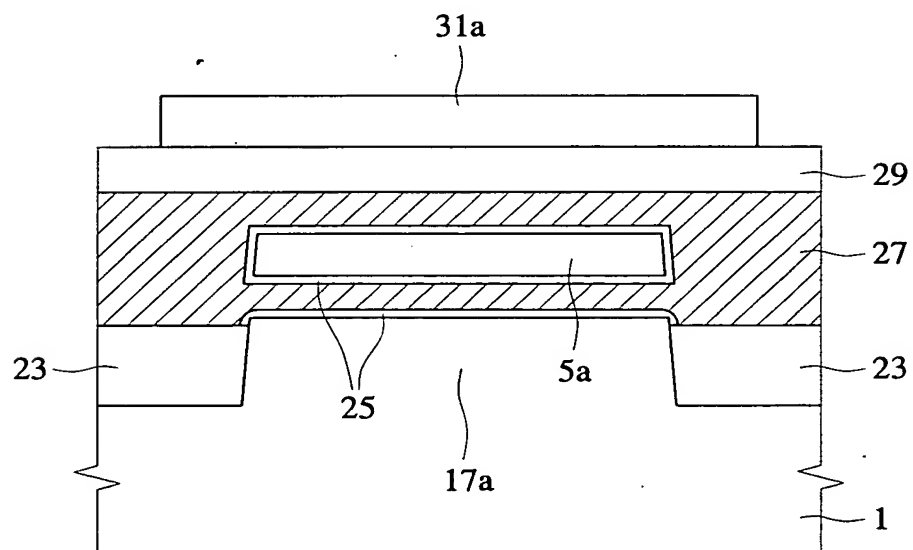




FIG. 9A

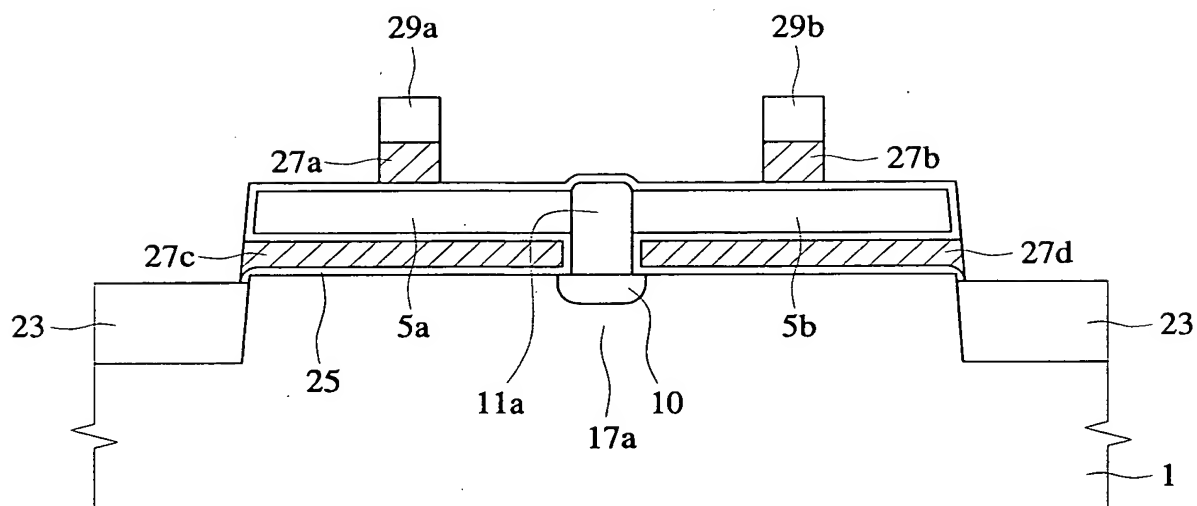
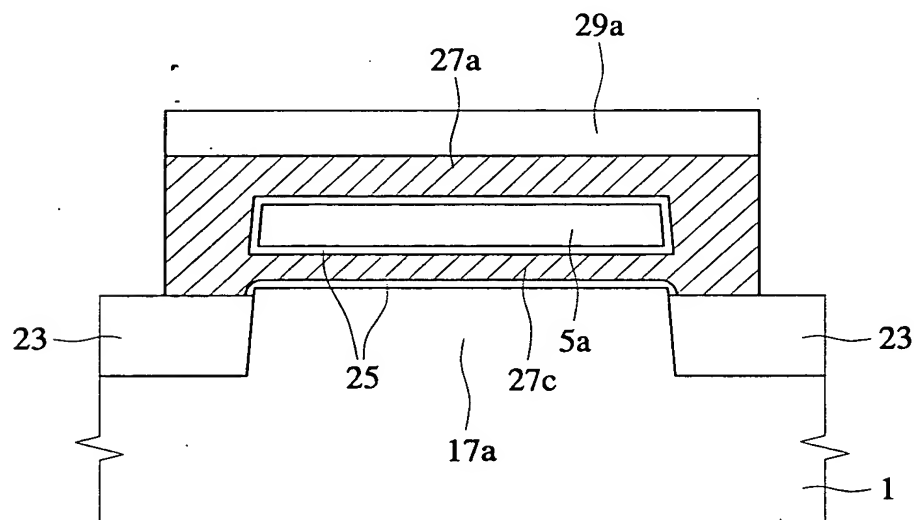


FIG. 9B



This cross-sectional view shows a semiconductor device with two semiconductor elements, 29a and 29b, mounted on a substrate 10. The elements are connected to a common bus 11a. The device includes various layers and structures, including a base layer 23, a layer 25, a layer 33, a layer 37c, and a layer 37d. The elements are connected to a common bus 11a, which is connected to a power source 1. The device also includes a layer 35a, a layer 35b, a layer 37a, and a layer 37b. The elements are connected to a common bus 11a, which is connected to a power source 1. The device also includes a layer 35a, a layer 35b, a layer 37a, and a layer 37b.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 1 with a well 23. A gate stack 25 is formed on the substrate, with a gate oxide 27a and a gate electrode 29a. A source/drain region 35b is formed on the gate stack, with a source/drain oxide 27c and a source/drain electrode 5a. The device is shown in a cross-sectional view with a central channel region 17a.

FIG. 10

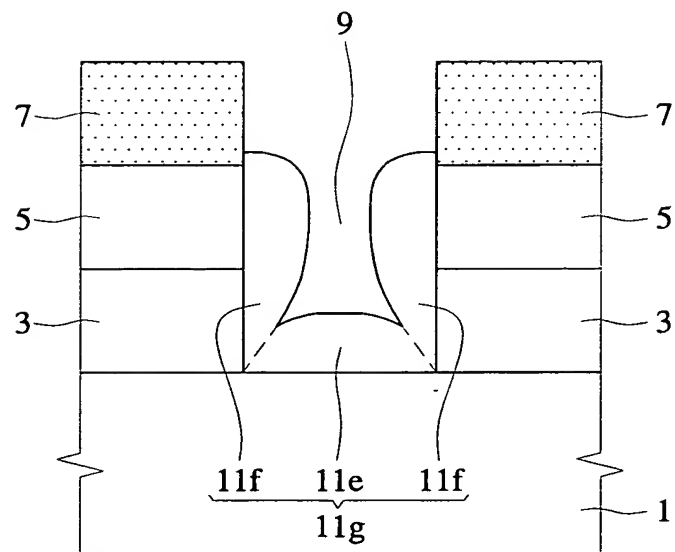


FIG. 11

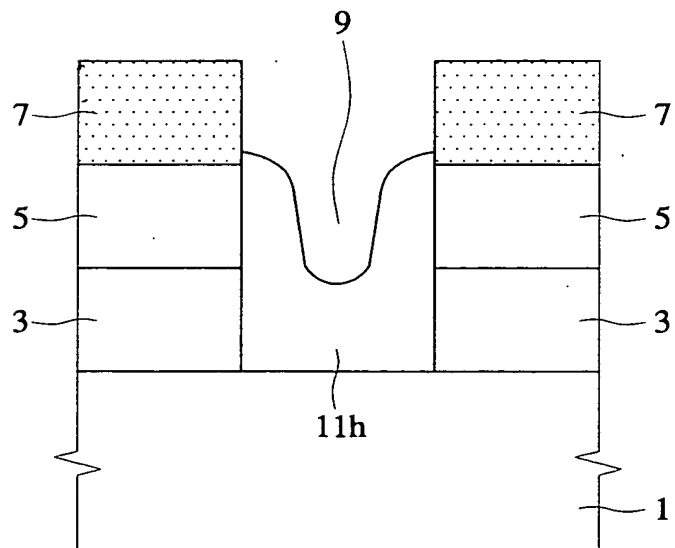


FIG. 13

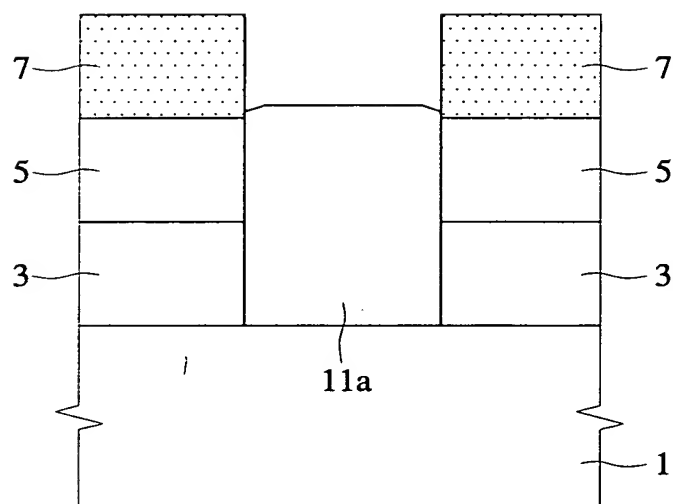


FIG. 14

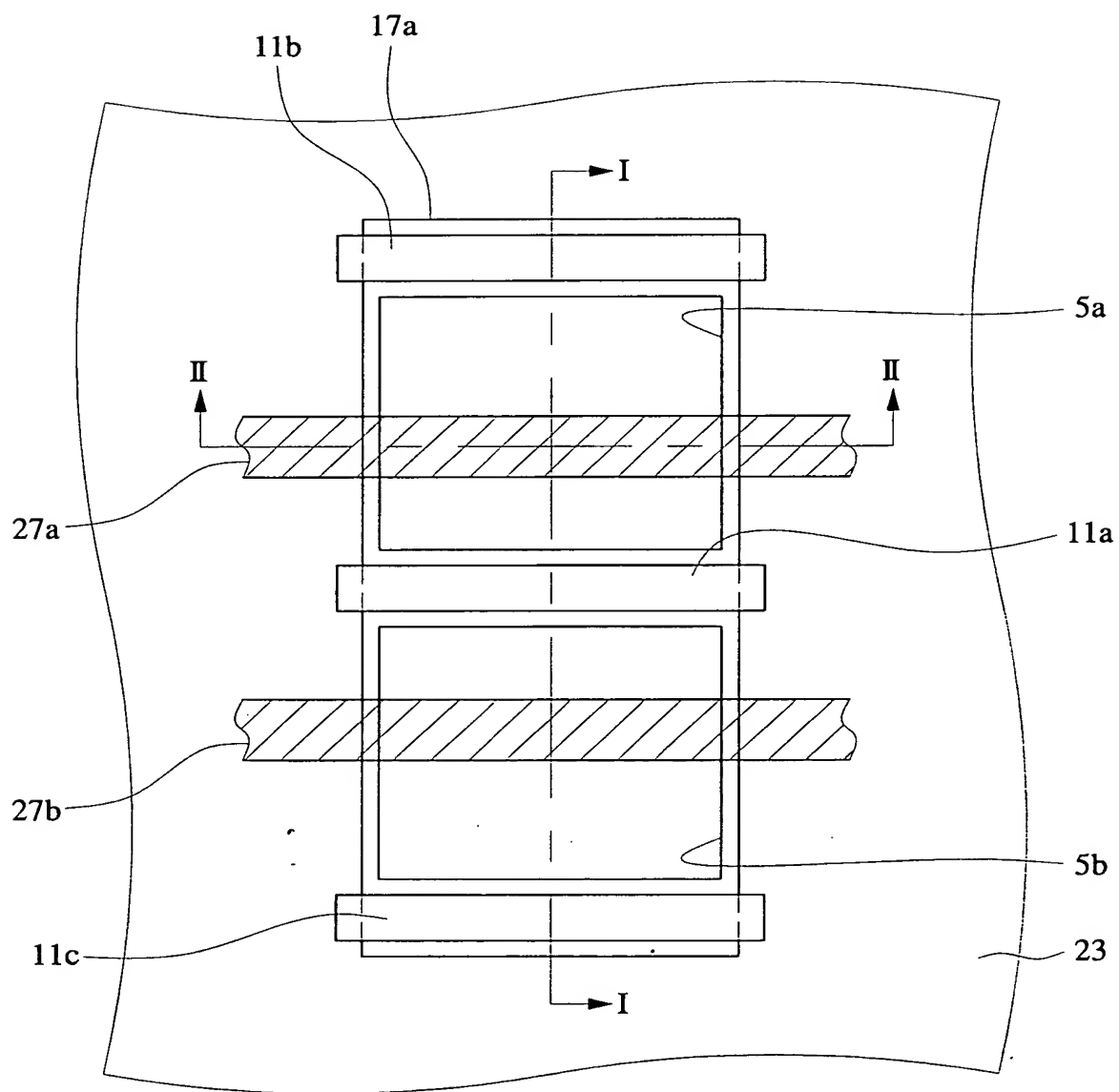


FIG. 15

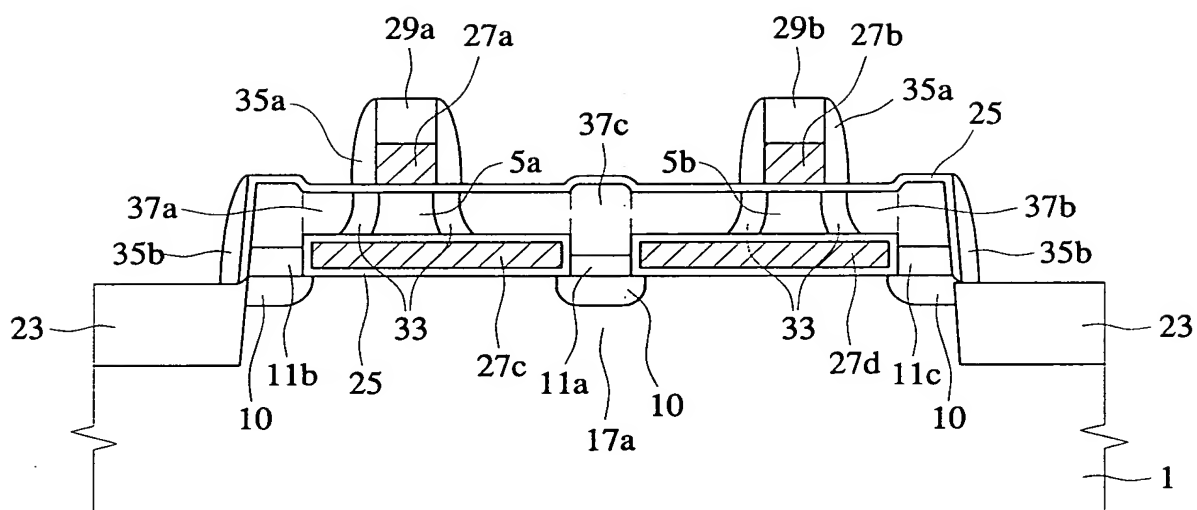


FIG. 16

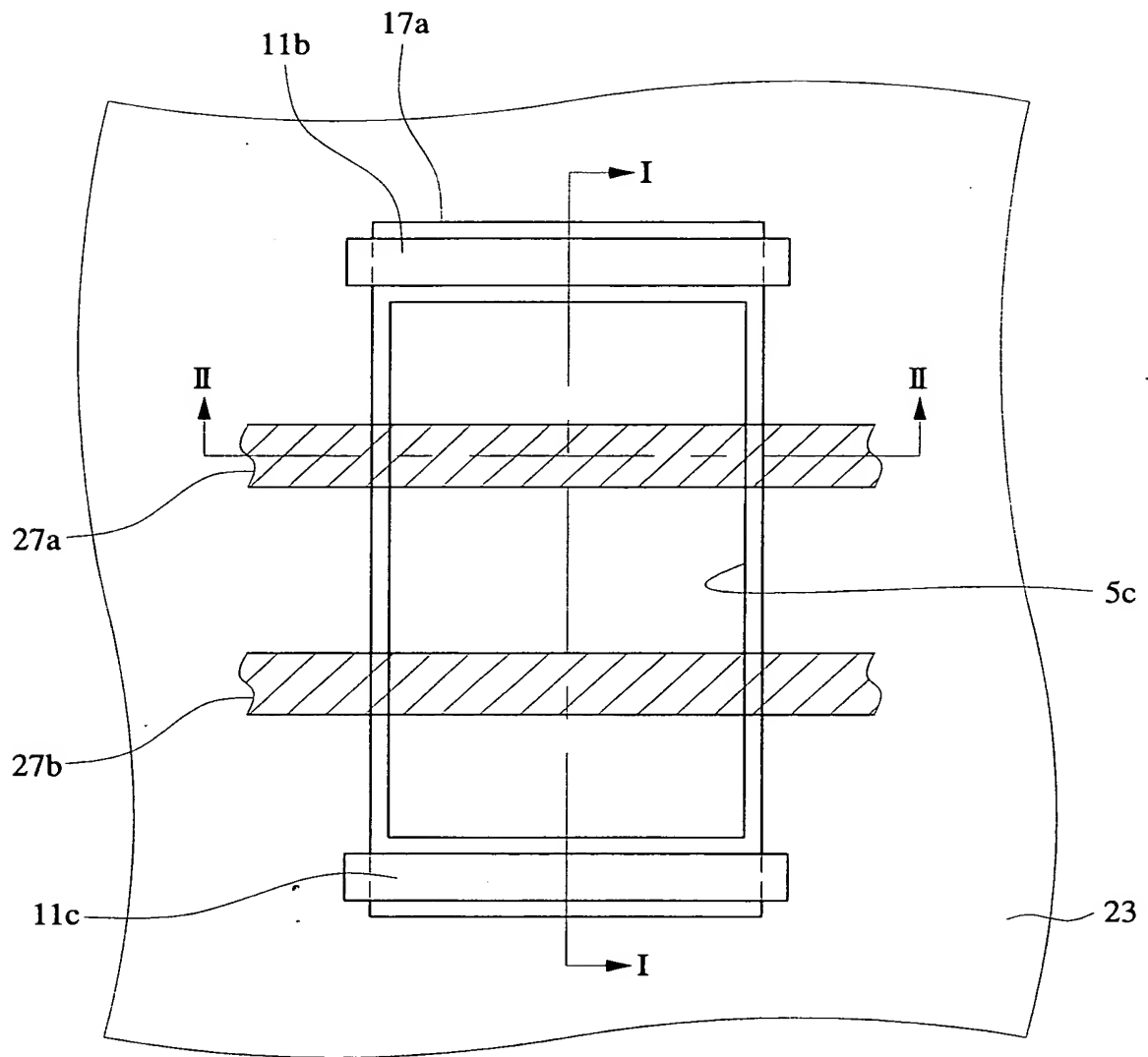


FIG. 17

